Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **BALANCE**
2. **–INPUT**
3. **+INPUT**
4. **–VS**
5. **OUTPUT**
6. **+VS**
7. **+VS**
8. **BALANCE**

**7**

**6**

**5**

**4**

**2 1 8**

**3**

**MASK**

**REF**

**843**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: ISOLATED**

**Mask Ref: 843**

**APPROVED BY: DK DIE SIZE .067” X .102” DATE: 3/26/19**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD843**

**DG 10.1.2**

#### Rev B, 7/1